REMARKS

This is intended as a full and complete response to the Final Office Action dated July 12, 2006, reconsideration and allowance of claims in requested.

In this office action, claims 1-20 are considered. Claims 1-10 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fraser (patent No. 6,907,598) in view of Mohamed (patent No. 6,684,319). Claims 11 and 12 which depend on Claim 1 are indicated to contain allowable subject matter but were objected to as being dependant upon a rejected base claim.

Applicants thank the examiner for the indication of allowable subject matter. Applicant hereby incorporates the limitation of Claim 10 into Claim 1. This combination does not create any issue after final as Claim 10 was previously directly dependant on Claim 1. Applicant further respectfully requests reconsideration of the other pending claims in view of the remarks below.

Applicants submit that Fraser and Mohamed either alone or in combination do not disclose or suggest every element of the independent claims. Moreover, there was no motivation to combine the two references, as their structure and approaches to the problem of executing a sequence of the instructions are fundamentally inconsistent with one another.

The Fraser patent '598 simply does not teach the claimed invention, as alleged by the examiner. Fraser identifies the problem of frequently executing a repeated subset of a total set of instructions. However, Fraser's approach to this problem is completely different than the claimed approach. Claim 1 states that a frequently executed instruction is identified. Then, an explicit caching instruction associating the identified instruction with an index value is inserted into the set of instructions and, finally, one instance of the frequently executed instruction is replaced with a compressed instruction. In contrast, Fraser simply identifies repeated sets of instructions found in the total stream of instructions. Then, for each subsequent execution of that stream of instructions, each repeated set of instructions is replaced with a single echo instruction, which is simply a pointer having a first parameter identifying the beginning of the set and a second perimeter identifying the end of the set (see column 9 lines 22 – 28). Thus, Fraser does

not insert a caching instruction and does not use an index value as described in the present application at page 14 and explicitly recited in the claims.

The Examiner relies on Mohamed to make up for this deficiency. However, as stated in column 3, line 35 – 55 of Mohamed, this reference uses a flag bit to indicate that a designated block of instructions is to be placed into a separate instruction buffer 114 instead of the instruction cache 110. This approach requires the addition of a separate instruction buffer 114, which is contrary to the teachings of the Fraser reference, which is explicitly directed to the problem of repeatedly executing the sequence of instructions within a single memory unit. Therefore, there is simply no motivation to adopt the approach of Mohamed and combine it with the teachings of Fraser. Moreover, Mohamed does not teach, and the Examiner does not allege that Mohamed teaches, replacing at least one instance of the frequently executed instructions with a compressed instruction. Instead, the Examiner at the top of page 8 of the office action (see the first three lines), returns to the echo instruction of Fraser. However, the Examiner has already relied on the echo instruction for teaching the limitation of inserting a caching instruction. He cannot rely on the exact same disclosure of the single echo instruction for also teaching the limitation of replacing the frequently executed instruction with a compressed instruction.

For these reasons, Claim 1 and its dependant claims as well as Claim 20, which includes these recitations, are allowable.

The same arguments apply to Claim 13 and the claims dependant thereon, although Claim 13 is written in a somewhat different format than Claim 1. Claim 13 also recites two different steps to be taken in executing the method (i.e., when the primary instruction is an explicit cache instruction, storing the instruction subsequent to the primary instruction in an instruction storage unit; and, when the primary instruction is a compressed instruction, retrieving from the instruction storage unit the one previously stored instruction using the compressed instruction). Against both of these limitations, the Examiner relies on the Mohamed reference for teaching a flag. However, a review of column 3, lines 34 – 60 of Mohamed illustrates that this reference does not teach two different operations depending on whether the primary instruction is an explicit cache instruction or a compressed instruction. Rather, Mohamed always operates the same

way, responding to a flag bit to capture a particular block of instructions and places the block into an instruction buffer. The flag is always decoded several instructions before the instructions are decoded, and the instructions are always transferred to the same region of memory 114. The alternate operations, depending on whether the primary instruction is the cache instruction or the compressed instruction, are not taught or suggested in Mohamed or in the Fraser reference, which also only teaches one kind of echo instruction that is limited to multiple executions of the same subset of instructions.

In view of these clear distinctions, reconsideration and allowance of all pending claims is respectively requested.

Respectfully submitted,

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